Faculty Profile

Name : Ms. Geetanjali Sharma

Designation : Assistant Professor

Qualifications : PhD pursuing, M.Tech, BE

Phone : 9999254316

Email : gsharma@msit.in

Area of Interest/Specialization: Electronic Devices, Biomedical Signal Processing, EEG signal processing, Digital VLSI, Low Power VLSI

Experience : 14 years

Key Publications

1. Sharma, Geetanjali, Abhishek Parashar, and Amit M. Joshi. "DepHNN: A novel hybrid neural network for electroencephalogram (EEG)-based screening of depression." *Biomedical Signal Processing and Control* 66 (2021): 102393.

2. Sharma, Sapna, Robinson Devasia, and Geetanjali Sharma. "A novel low power and highly efficient inverter design." *International Journal of Information Technology* 12, no. 4 (2020): 1111-1116.

3. Arora, Harmeet Singh, Rohan Kochar, and Geetanjali Sharma. "High Performance Implementation of Universal Gate using Low Power Source Gating Technique." *International Journal of Computer Applications* 96, no. 10 (2014).

4. Handa, Ankish, Prateek Garg, and Geetanjali Sharma. "A Novel Power Reduction Technique for CMOS Circuits using Voltage Scaling and Transistor Gating." *International Journal of Computer Applications* 92, no. 11 (2014).

5. Handa, Ankish, Paanshul Dobriyal, and Geetanjali Sharma. "A Novel High Performance Low power universal Gate implementation in subthreshold region." *International Journal of Computer Applications* 87, no. 12 (2014).

6. Rajput, Navya, Ankit Jindal, Sahil Saroha, Ritesh Kumar, and Geetanjali Sharma. "A novel and high performance implementation of 8x8 multiplier based on vedic mathematics using 90nm hybrid ptl/cmos logic." *International Journal of Computer Applications* 69, no. 27 (2013).

7. Sharma, Karna, Manan Sethi, Paanshul Dobriyal, and Geetanjali Sharma. "Designing a Novel Power Efficient D-Flip Flop using Forced Stack Technique." *International Journal of Computer Applications* 975 (2013): 8887.

8. Suri, Lakshay, Devesh Lamba, Kunwar Kritarth, Bhavna Ghai, and Geetanjali Sharma. "Design of High Performance and Power Efficient 16-bit Square Root Carry Select Adder using Hybrid PTL/CMOS Logic." *International Journal of Computer Applications* 69, no. 10 (2013).

9. Sethi, Manan, Karna Sharma, Paanshul Dobriyal, Navya Rajput, and Geetanjali Sharma. "A Novel High Performance Dual Threshold Voltage Domino Logic Employing Stacked Transistors." *International Journal of Computer Applications* 77, no. 5 (2013): 30-35.

10. Sharma, Geetanjali, Uma Nirmal, and Yogesh Misra. "A low power 8-bit magnitude comparator with small transistor count using hybrid ptl/cmos logic." *IJCEM International Journal of Computational Engineering & Management* 12 (2011): 2230-7893.

11. Nirmal, Uma, Geetanjali Sharma, and Yogesh Mishra. "A low power high speed adders using MTCMOS Technique." *IJCEM International Journal of Computational Engineering & Management* 13 (2011).

12. Rajput, Navya, Manan Sethi, Karna Sharma, Paanshul Dobriyal, and Geetanjali Sharma. "A Novel, High Performance and Power Efficient Implementation of Decimal to BCD Converter using 90nm Hybrid PTL/CMOS Technique."

Papers presented in Conferences

1. Thakur, Saurabh, Yajash Goplani, Sahil Arora, Rohit Upadhyay, and Geetanjali Sharma. "Chest X-Ray Images Based Automated Detection of Pneumonia Using Transfer Learning and CNN." In *Proceedings of International Conference on Artificial Intelligence and Applications*, pp. 329-335. Springer, Singapore, 2021.

2. Devasia, Robinson, Yashi Sarbhai, and Geetanjali Sharma. "Comparative analysis of ecrl and tsel adiabatic logic styles." In *2018 International Conference on Current Trends towards Converging Technologies (ICCTCT)*, pp. 1-6. IEEE, 2018.

3. Handa, Ankish, Jitesh Chawla, and Geetanjali Sharma. "A novel high performance low power CMOS NOR gate using Voltage Scaling and MTCMOS technique." In *2014 International Conference on Advances in Computing, Communications and Informatics (ICACCI)*, pp. 624-629. IEEE, 2014.

4. Dobriyal, Paanshul, Karna Sharma, Manan Sethi, and Geetanjali Sharma. "A high performance d-flip flop design with low power clocking system using mtcmos technique." In *2013 3rd IEEE International Advance Computing Conference (IACC)*, pp. 1524-1528. IEEE, 2013.

5. Rajput, N., M. Sethi, P. Dobriyal, K. Sharma, and G. Sharma. "A novel, high performance and power efficient implementation of 8× 8 multiplier unit using MT-CMOS technique." In *2013 Sixth International Conference on Contemporary Computing (IC3)*, pp. 186-191. IEEE, 2013.

6. Suri, Lakshay, Devesh Lamba, Kunwar Kritarth, and Geetanjali Sharma. "High performance and power efficient 32-bit carry select adder using hybrid PTL/CMOS logic style." In *2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s)*, pp. 765-768. IEEE, 2013.

7. Sharma, Geetanjali, Uma Nirmal, and Yogesh Mishra. "Comparative Analysis of High Performance Full Subtractor using Hybrid PTL/CMOS Logic." In *proceeding of International Conference on Advances in Information Communication Technology and VLSI Design, Coimbatore, India*. 2010.

8. Sharma, Geetanjali, Uma Nirmal, and Yogesh Mishra. "Synthesis of Hybrid PTL/CMOS Logic for Low Area/Power Applications." In *proceeding of International Conference on System Dynamics and Control, India*. 2010.

Total Citations: 145
h-index: 8
i-10 index: 6

Awards and Recognitions

1. **Best Paper Award** for "Comparative Analysis of High Performance Full Subtractor using Hybrid PTL/CMOS Logic" in IEEE International Conference on Advances in Information Communication Technology and VLSI Design, Coimbatore, India.

Patent/Copyright

1. Ms. Geetanjali Sharma has published Patent on "Method and Electronic device for monitoring user in work" in 2021.

Sponsored Project/Consultancy

1. Adopted "Nagali Jalib" (2018-2021) for its technological and social development under Unnat Bharat Abhiyaan (UBA), a flagship program of the Ministry of Education (MHRD), Government of India.

Book Chapter/Book Published

1. High-Performance Comparator Design using Hybrid PTL/CMOS Logic Style, Lambert Academic Publishing, Germany.

Memberships of Professional bodies

1. IEEE
2. Lifetime Member with ISTE
3. Faculty Coordinator of IEEE signal processing society

Other Contributions:

1. In charge of Institute Industry Interaction cell (III Cell) since the year 2017 and organising several Summer/ Winter Training Programs for the students of MSIT.
2. Providing Internship opportunities to the students.
3. Set up Electronic Devices Lab in ECE Department.
4. Part of Unnat Bharat Abhiyan (UBA) a flagship program of the Ministry of Education (MHRD), Government of India.
5. Proctor faculty of FDP on "ICT Tools for Teaching, Learning process & Institutes (10 to 21 Aug2020) organized at MNIT.